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rtl compil\* path

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S Design, V Netlist, RTLC Prepare, C Design - ics.ele.tue.nl

 ... Besides this so-called data **path** architecture, a controller description is constructed to control the data flow in the architecture. ...

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[Optimized generation of data-path from c codes for fpgas](#)

 Z Guo, B Buyukkurt, W Najjar, K Vissers - Design, Automation and Test in Europe, 2005. Proceedings, 2005 - [ieeexplore.ieee.org](#)

 ... 3. Section 4 presents ROCCC compiler **RTL** code generation for the controller, the buffer and the data **path**. ... ROCCC's objective is to **compile** these kernels to ...

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 O Schliebusch, A Chattopadhyay, EM Witte, D ... - Rapid System Prototyping, 2005.(RSP 2005). The 16th IEEE ..., 2005 - [ieeexplore.ieee.org](#)

 ... which refer to the data **path** of the ... A **compile**-time conditional statement contains a condition ... The optimizations performed during **RTL** processor synthesis from ...

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[RTL emulation: the next leap in system verification](#)

 S Sawant, P Giordano - Proceedings of the 33rd annual conference on Design ..., 1996 - [portal.acm.org](#)

 ... Control logic and data-**path** optimization are handled by different algorithms. ... **RTL**

 Reader System-level Sign-off **Compile** Clock Analysis Automatic Partition ...

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 BY Start, C Compilation - [asic.ee.cuhk.edu.hk](#)

 ... longer to **compile** but can produce better designs. The mapping process proceeds until it has tried all strategies. This setting enables critical **path** resynthesis ...

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 S Family - [ins.clrc.ac.uk](#)

 ... Overview of Mentor's FPGA Design Flow ■ Introduction To Precision **RTL** Synthesis ...

 ITA will provide new **path** information ... **compile** and copied to the ...

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 ZGBBW Najjar, K Vissers - [arxiv.org](#)

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E Botcazou, C Comar, O Hainque - GCC Developers' Summit - gccsummit.org

... as the sum of the values associated with each node on the **path**. ... we also try to deduce from the IL (here **RTL**) limits easily evaluated at **compile-time**. ...

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### A comprehensive pre-RTL IC design methodology

PP Jain, CAEP Inc, TX Austin - 1995 IEEE International Verilog HDL Conference, 1995. ..., 1995 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... the external behavior of the data **path** elements and ... Synthesis Behavioral synthesis tools **compile** algorithmic descriptions into **RTL** descriptions. ...

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SY Cheng - [acar.ee.nctu.edu.tw](mailto:acar.ee@nctu.edu.tw)

... **compile** ... 2. Read in design • Read in the **RTL** verilog source files Page 18. ... Report – min/max delay **path** – constraints violations (area, timing, power) ...

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